REMARKS

Claims 1-29, all the claims pending in the application, stand rejected. Applicant has amended claim 7 in order to state the invention in conventional method claim form.

Claim Rejections - 35 U.S.C. §102

Claim 7 is rejected under 35 U.S.C. §102(b) as being anticipated by Igarashi (5,740,462). This rejection is traversed for at least the following reasons.

The Examiner asserts that Igarashi discloses a font data reading method as claimed. In particular, the Examiner refers to Fig. 2, which illustrates the content of a font management table, and identifies element 205 as being an address specifying a font and element 203 as the being data identifying a basic resolution. Further, element 120 in Fig. 1 is considered the input terminals for specifying the font and resolution, and element 107 is considered as the storage medium having different font and resolution. Element 107 is identified as a "font table" that is coupled to a CPU 102, which serves to receive input character and resolution data (120) and is coupled to a character generator 103, font memory 108 and image memory 104 in controlling a font generation and output function for an image forming device 106.

Claim 7 is written in a narrative, rather than conventional method form. Thus, Applicant suspects that the claim has not been properly interpreted in a manner that considers the patentable features of the invention. Accordingly, Applicants have revised claim 7 in order to better state the invention. On this basis, Applicant respectfully submits that the claim is distinguishable over the reference.

In particular, as detailed subsequently with respect to the product claims in the application, the patent to Igarashi does not teach a method related to a font memory, as claimed.

Claim Rejections - 35 U.S.C. §103

Claim 1 is rejected under 35 U.S.C. §103(a) as being unpatentable over Igarashi (5,740,462). This rejection is traversed for at least the following reasons.

The invention of claim 1, particularly with reference to Fig. 1 of the present application, is directed to a font memory in which a plurality of groups of font data, having (1) different

resolutions and (2) represented by dot patterns, are stored for respective character codes. The font memory of a first embodiment, as illustrated in Fig. 1, includes a plurality of first input terminals for character-specifying address signals (A_0A_x) and a plurality of second input terminals for specifying resolution levels (L_0-L_z). In addition, there are a plurality of output terminals for delivering stored font data (D_0-D_y). Significantly, the claim states that on the basis of the character specifying address and font resolution level, font data is output from the font memory.

As is clear from Fig. 1, in the language of the rejected claim, the invention is a "font memory 10". The font memory does not include a processor, I/O interface, bust, controller or the like. As explained at page 9 of the present application, the data stored in the memory corresponding to each character code of many bit map fonts will include font data for each of a plurality of resolution levels of the fonts for each character code. The specification states at page 9, line 22 that:

> "For example, assume that there are 3,000 characters (types of characters) in one character code, three types of fonts, and each font has 5 resolution levels. In this case, bit map font data of amount 3,000 x 3 x 5 is stored in the font memory 10."

As explained at page 10, line 19, the input signals specifying the character address identify the storage area (the memory cell group) that contain a font pattern determined by the font type and character code. The font resolution level signal specifies the resolution level from among the font patterns specified by the character specifying address.

The remaining disclosure at pages 10-15 describes a first embodiment of such font memory, including the capability for outputting font data of variable resolutions and size. The advantage of such storage is reduced access time, as explained at page 14, line 4. The font memory in accordance with the second embodiment is disclosed beginning at page 14, line 19, with regard to Fig. 3 and a third embodiment is disclosed at page 17, line 6, with regard to Fig. 4. A fourth embodiment is described at page 18 with regard to Fig. 5.

The concept of using character structure specifying addresses is explained with regard to Fig. 6 and the structure of a character structure address output from a font memory 40 is explained with regard to Figs. 7(a) and 7(b).

Igarashi

The patent to Igarashi discloses a system for generating output images on line 121 of Fig. 1, as noted by the Examiner. The system 100 includes an input 120 and interface 101, a CPU 102, character generator 103, output interface 105 and a variety of memory devices coupled to the CPU 102, including an image memory 104, font table 107, font memory 108 and non-volatile memory 112. Clearly, the overall system 100 is not a "font memory," as claimed. This is precisely the type of CPU-based character generation system that Applicant distinguished at page 14, line 4 of the present application in emphasizing the advantages of the present invention.

Moreover, none of the individual memory devices (107, 108, 112) disclosed by Igarashi can meet the font memory limitations specified in the claim. In the absence of such structure, the rejection of the claim as being unpatentable over Igarashi is clearly overcome.

Claim 2 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Igarashi (5,740,462) and further in view of Sugiura et al (5,189,523). This rejection is traversed for at least the following reasons.

Again, claim 2 is directed to a "font memory" having a plurality of first input terminals, first output terminals and second output terminals, such that the claim covers at least the embodiment illustrated in Fig. 3. The claim specifies that the resolution level is "sequentially altered at a predetermined timing" and further specifies that font data corresponding to a character code and resolution signals representing a resolution level are output from the terminals.

As already noted, Igarashi concerns a system and not a font memory. Therefore, Igarashi is not directed to the subject matter of the claim. Further, the Examiner admits that Igarashi does not explicitly disclose "the resolution level is sequentially altered at a predetermined timing, in addition to font data corresponding to the character specified by the character specifying address

signals and corresponding to the resolution level being output from said first output terminals, resolution signals representing the resolution level are output from said second output terminals".

The Examiner looks to Sugiura et al for the disclosure of a method of display image in which resolution of an image is incremented sequentially by address counter, with reference to col. 13, line 37-39.

However, Sugiura does not remedy the deficiencies of Igarashi in that it does not teach how the system of Igarashi may be implemented as a font memory, as claimed. Moreover, Sugiura itself discloses an image processing apparatus that is an image capturing device, particularly useful for a color copier. In capturing images, it must discriminate a characteristic of the image, such as characters vs. halftones. Sugiura is not concerned with a font memory.

Sugiura does illustrate in Fig. 7 a bit map memory 7-1 that corresponds to the bit-map memory 3-1 in Fig. 3. As illustrated in Fig. 3, the bit map memory receives address inputs from counter 3-11 as well as inputs D0-D7, and outputs to an image processing circuit 3-12. As detailed in Fig. 7 and explained at col. 7, line 31-col. 8, line 28, , the bit map memory 7-1 receives address inputs at input A0 as well as image discrimination signals (D0, D1) and a variety of area signals AR2-AR7. Though not discussed, the bit map memory would appear to be read out conventionally, by address input. However, nothing in the disclosure teaches the features of a font memory, as claimed.

In sum, the apparatus permits one to designate an area in order to decrease misjudgments about the image discrimination signals, and is structured in such a way that the result of AND-ing or OR-ing of the area designation information with the image description information can be written into the bit map memory. However, this function of the disclosed bit map memory 7-1 does not meet the claim limitations.

Claims 3 and 8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Igarashi (5,740,462) in view of Sugiura et al and further in view of Suzuki (JP 4-10290367). This rejection is traversed for at least the following reasons.

As a preliminary matter, Applicant notes that claim 3 is dependent from claim 1 and claim 8 is dependent from claim 2. Thus, these claims should be allowable for the reasons already given with regard to the patentability of those claims. Further, the Examiner admits that Igarashi and Sugiura do not explicitly disclose "based on the number of dots in the dot pattern, a density level is calculated when the dot pattern is displayed and density level signal specifying the calculated density level are output from said density level output terminals." The Examiner looks to Suzuki for an image processor in which pixel calculation unit calculates the output density of the sub pixel of an input image signal based on a dot pattern.

As already noted, neither Igarashi nor Sugiura concern a font memory as claimed in claims 1 and 2. Suzuki does not remedy this deficiency as, by the Examiner's own admission, it concerns a system where a processor is used to calculate a density level when the dot pattern is displayed.

The rejected claims are directed to a post memory output feature of the invention. Even if Suzuki teaches such processor operation, there is no teaching or suggestion in Suzuki that would cause Igarashi and Sugiura to be modified such that they disclose the basic font memory as claimed. Thus, this rejection is overcome.

Claims 4 and 9-11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Igarashi in view of Sugiura and Suzuki et al and further in view of Rider et al (4,152,697). This rejection is traversed for at least the following reasons.

These claims depend from claims 1, 2, 3 and 8 and would be patentable for the reasons already given with regard to those claims. Further, the Examiner admits that Igarashi, Sugiura and Suzuki do not explicitly disclose "an exclusive address given to each dot forming the dot pattern and the font data is information representing the dot pattern using the address exclusive to a particular dot." The Examiner asserts that this is taught by Rider et al, particularly with regard to the font memory in Figs. 1-16 where "in the matrix format one bit is stored for each dot or element of the character." (Col. 2, lines 37-39).

Notwithstanding this description in Rider, the fundamental flaw in the Examiner's analysis has not been remedied. Rider does not teach how any of the other three references

combined to formulate this rejection may be modified such that they are directed to a font memory. Moreover, the font memory 16, as illustrated in Fig. 1 of Rider, is adapted to store characters in either a matrix format or run length format or run length incremental format (col. 2 line 32). However, there is no teaching or suggestion with regard to the storing of a plurality of font data with different resolution. Thus, this additional sophisticated feature of the present invention is not contemplated at all by Rider et al. Accordingly, these claims should be considered allowable over the combination of references cited by the Examiner.

Claims 5-6 and 12-29 are rejected under 35 U.S.C. §103(a) as being unpatentable over Igarashi (5,740,462) in view of Sugiura and Suzuki, and further in view of Ogino et al (6,593,902). This rejection is traversed for at least the following reasons.

As a preliminary matter, Applicant notes that these claims depend from claims 1-3 and 8-11, which have been demonstrated to be patentable. Further, the Examiner admits that Igarashi does not explicitly disclose the limitation "wherein the dot pattern is divided by a first division unit into a plurality of pattern areas, a relevant pattern address for identifying the area as allocated to each of the created pattern areas, each pattern area divided by the first division unit is further divided by a second division unit into a plurality of pattern areas, and an address for identifying the relevant pattern area as allocated to each of the pattern areas created using the second division unit, and wherein the font data is information representing the dot pattern using the addresses obtained by repeating the above division and address allocation thereafter for an optional number of times." This is a further reason why the present invention is distinguishable over Igarashi, Sugiura and Suzuki.

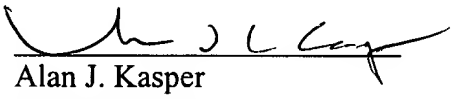
With regard to Ogino, the reference is deficient in failing to remedy the deficiencies of Igarashi, Sugiura and Suzuki, as already demonstrated. Further, the Examiner asserts that Ogino discloses the method of addresses displayed information in which the displayed area is divided and addressed until an appropriate level (Fig. 8A-8D) is achieved.

On the basis of the foregoing arguments and the proposed amendment to claim 7, we believe that all the claims would be patentable over the several items of prior art cited by the Examiner, taken alone or in combination. .

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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23373
CUSTOMER NUMBER

Date: November 9, 2004